Amendments to the Claims:

(Claim 1) 1. (Currently Amended) A trans_impedance filter circuit processing an input signal and generating an output signal, said trans_impedance filter circuit comprising:

an operational amplifier having an inverting input terminal, a non_inverting input terminal and an output path;

a first resistor having one terminal coupled to receive said input signal, and another terminal being coupled to said inverting input terminal;

a first capacitor being coupled between said one terminal of said first resistor and a first constant bias;

a second resistor connected between a first node and said output path, wherein said first node is in a path said input signal is provided to said inverting input terminal; and

a second capacitor connected between said inverting input terminal and said output path[[.]]; further comprising:

a third resistor connected in series with said first resistor at a second node, wherein said another terminal of said third resistor is connected to receive said input signal at said first node;

a third capacitor and a fourth capacitor connected in series between said first node and said inverting input terminal, said third capacitor being connected to said fourth capacitor at a third node; and

a fourth resistor being connected between said third node and a third constant bias.

(Claim 2) (Cancelled)

(Claim 3) 3. (Currently Amended) The trans_impedance filter circuit of claim [[2]]1, further comprising a fifth capacitor connected between said output path and said second node.

(Claim 4) 4. (Original) The trans_impedance filter circuit of claim 3, wherein said first capacitor has a capacitor of 2kC(1-ë) said fifth capacitor has a capacitance of 2kCë and said fourth resistor has a resistance equaling kR/2, wherein C represents the capacitance of each of said third capacitor and said fourth capacitor, R represents the resistance of said first resistor, k and ë are variables which can be set by a designer to attain desired filter characteristics.

(Claim 5) 5. (Original) The trans_impedance filter circuit of claim 4, wherein said trans_impedance filter circuit is implemented in a differential mode, and said output path comprises an inverting output terminal and a non_inverting output terminal.

(Claim 6) 6. (Original) The trans_impedance filter circuit of claim 5, wherein said fifth capacitor is connected between said second node and said non_inverting output terminal to attain a positive value for said ë.

(Claim 7) 7. (Original) The trans_impedance filter circuit of claim 5, wherein said fifth capacitor is connected between said second node and said inverting output terminal to attain a negative value for said ë.

(Claim 8) 8. (Current Amended) A device comprising:

a trans_impedance filter circuit processing an input signal and generating an output signal, said trans_impedance filter circuit comprising:

an operational amplifier having an inverting input terminal, a non_inverting input terminal and an output path, said output path providing said output signal;

a first resistor having one terminal coupled to receive said input signal, and another terminal being coupled to said inverting input terminal;

a first capacitor being coupled between said one terminal of said first resistor and a first constant bias;

a second resistor connected between a first node and said output path, wherein said first node is in a path said input signal is provided to said inverting input terminal; and

a second capacitor connected between said inverting input terminal and said output path; and

an analog to digital converter coupled to said output path, and sampling said output signal to generate a plurality of digital samples[[.]]; further comprising:

a third resistor connected in series with said first resistor at a second node, wherein said another terminal of said third resistor is connected to receive said input signal at said first node;

a third capacitor and a fourth capacitor connected in series between said first node and said inverting input terminal, said third capacitor being connected to said fourth capacitor at a third node; and

a fourth resistor being connected between said third node and a third constant bias.

(Claim 9) (Cancelled)

(Claim 10) 10. (Currently Amended) The device of claim [[9]]8, further comprising a fifth capacitor connected between said output path and said second node.

(Claim 11) 11. (Original) The device of claim 10, wherein said first capacitor has a capacitance of 2kC(1- ë) said fifth capacitor has a capacitance of 2kCë and said fourth resistor has a resistance equaling kR/2, wherein C represents the capacitance of each of said third capacitor and said fourth capacitor, R represents the resistance of said first resistor, k and ë are variables which can be set by a designer to attain desired filter characteristics.

(Claim 12) 12. (Original) The device of claim 11, wherein said trans_impedence filter circuit is implemented in a differential mode, and said output path comprises an inverting output terminal and a non_inverting output terminal.

(Claim 13) 13. (Original) The device of claim 12, wherein said fifth capacitor is connected between said second node and said non_inverting output terminal to attain a positive value for said ë.

(Claim 14) 14. (Original) The device of claim 12, wherein said fifth capacitor is connected between said second node and said inverting output terminal to attain a negative value for said ë.

(Claim 15) 15. (Currently Amended) The device of claim [[9]]8, further comprising:

a low noise amplifier receiving an external signal at a carrier frequency and generating an amplified signal; and

a mixer down-converting said amplified signal to generate said input signal with the frequency band of interest being centered at a lower frequency than the carrier frequency.